Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns,

wherein each of the non-volatile memory devices has:

a word gate formed above a semiconductor layer with a gate insulating layer interposed;

an impurity layer formed in the semiconductor layer to form a source region or a drain region; and

control gates in the form of side walls formed along both side surfaces of the word gate,

wherein each of the control gates consists of a first control gate and a second control gate adjacent to each other;

wherein a first insulating layer which is a stack of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film is disposed between the first control gate and the semiconductor layer, and a side insulating layer is disposed between the first control gate and the word gate;

wherein a second insulating layer which is a stack of a silicon oxide film and a silicon nitride film is disposed between the second control gate and the semiconductor layer; and

wherein the thickness of the silicon nitride film of the second insulating layer is less than the thickness of the silicon nitride film of the first insulating layer.

2. (Original) The semiconductor device as defined in claim 1,

wherein a charge transfer protection film is formed on the second insulating layer.

3. (Original) The semiconductor device as defined in claim 2,

wherein the charge transfer protection film is one of a silicon oxide film and a silicon nitride oxide film.

4.-8. (Canceled)